FUJITSU SEMICONDUCTOR
DATA SHEET

DS05–20807–3E

FLASH MEMORY

CMOS

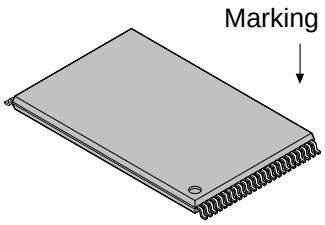
16 M (2 M × 8) BIT

MBM29F016 - 90/-12

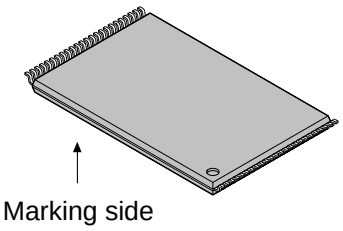
■ DISTINCTIVE CHARACTERISTICS

- **Single 5.0 V read, write, and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  Pinout and software compatible with single-power supply Flash
  Superior inadvertent write protection
- **48-pin TSOP**
- **Minimum 100,000 write/erase cycles**
- **High performance**
  90 ns maximum access time
- **Sector erase architecture**
  Uniform sectors of 64K bytes each
  Any combination of sectors can be erased. Also supports full chip erase.
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically programs and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/BUSY output (RY/BY)**
  Hardware method for detection of program or erase cycle completion
- **Low power consumption**
  40 mA maximum active read current
  60 mA maximum program/erase current
- **Enhanced power management for standby mode**
  <1 μA typical standby current
  Standard access time from standby mode
- **Low Vcc write inhibit ≤ 3.2 V**
- **Hardware RESET pin**
  Resets internal state machine to the read mode
- **Erase Suspend/Resume**
  Supports reading or programming data to a sector not being erased
- **Sector group protection**
  Hardware method that disables any combination of sector groups from write or erase operation (a sector group consists of 4 adjacent sectors of 64K bytes each)

■ PACKAGE



FPT-48P-M19



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■ GENERAL DESCRIPTION

The MBM29F016 is a 16M-bit, 5.0 V-Only Flash memory organized as 2M bytes of 8 bits each. The 2M bytes of data is divided into 32 sectors of 64K bytes for flexible erase capability. The 8 bit of data will appear on DQ0 to DQ7. The MBM29F016 is offered in a 48-pin TSOP package. This device is designed to be programmed in-system with the standard system 5.0 V VCC supply. A 12.0 V VPP is not required for program or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard MBM29F016 offers access times between 90 ns and 120 ns allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The MBM29F016 is command set compatible with JEDEC standard single-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The MBM29F016 is programmed by executing the program command sequence. This will invoke the Embedded Program™ Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Each sector can be programmed and verified in less than 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase™ Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

This device also features a sector erase architecture. The sector erase mode allows for sectors of memory to be erased and reprogrammed without affecting other sectors. A sector is typically erased and verified within one second (if already completely preprogrammed). The MBM29F016 is erased when shipped from the factory.

The MBM29F016 device also features hardware sector group protection. This feature will disable both program and erase operations in any combination of eight sector groups of memory. *A sector group consists of four adjacent sectors grouped in the following pattern: sectors 0-3, 4-7, 8-11, 12-15, 16-19, 20-23, 24-27, and 28-31.*

Fujitsu has implemented an Erase Suspend feature that enables the user to put erase on hold for any period of time to read data from or program data to a non-busy sector. Thus, true background erase can be achieved.

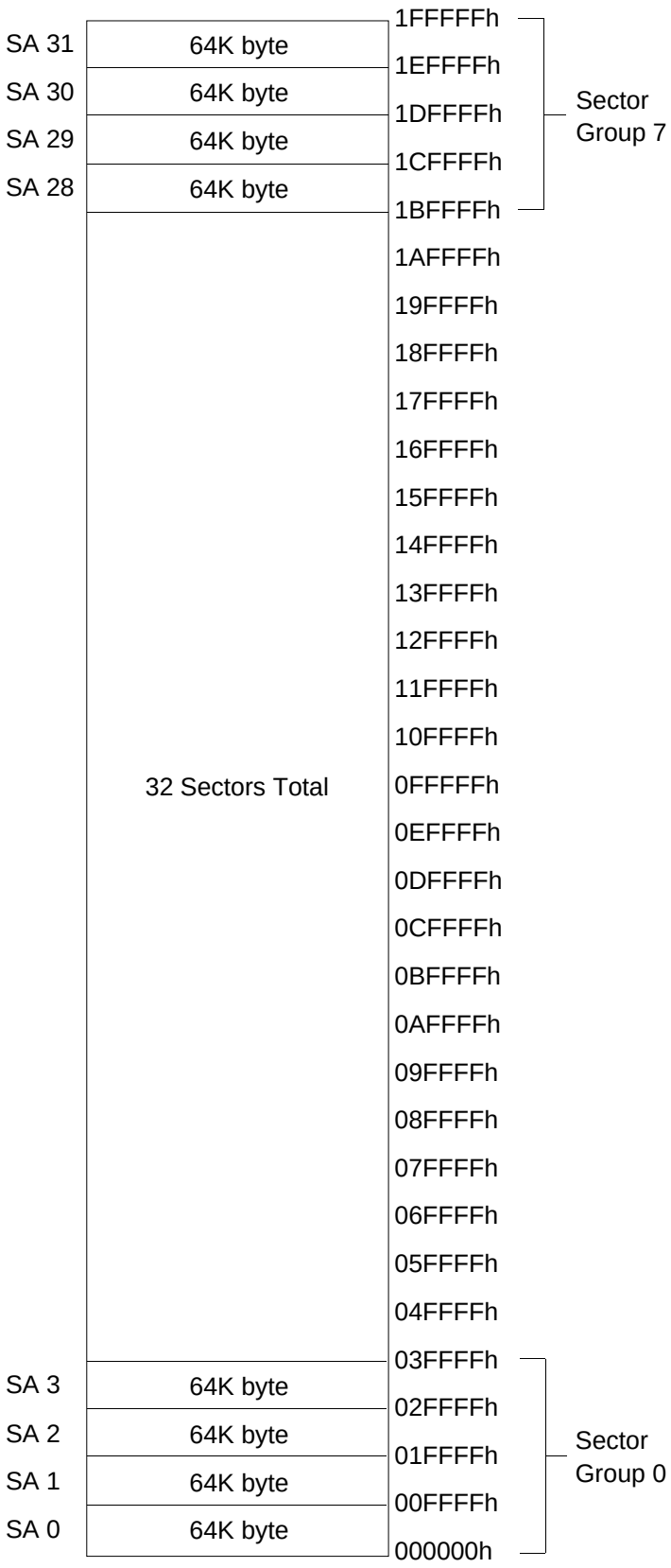
The device features single 5.0 V power supply operation for both read and program functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during power transitions. The end of program or erase is detected by $\overline{Data}$ Polling of DQ_7, or by the Toggle Bit I feature on DQ_6 or RY/$\overline{BY}$output pin. Once the end of a program or erase cycle has been completed, the device automatically resets to the read mode.

The MBM29F016 also has a hardware $\overline{RESET}$ pin. When this pin is driven low, execution of any Embedded Program or Embedded Erase operations will be terminated. The internal state machine will then be reset into the read mode. The $\overline{RESET}$ pin may be tied to the system reset circuity. Therefore, if a system reset occurs during the Embedded Program or Embedded Erase operation, the device will be automatically reset to a read mode. This will enable the system microprocessor to read the boot-up firmware from the Flash memory.

Fujitsu's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29F016 memory electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- Thirty two 64K byte sectors
- 8 sector groups each of which consists of 4 adjacent sectors in the following pattern; sectors 0-3, 4-7, 8-11, 12-15, 16-19, 20-23, 24-27, and 28-31
- Individual-sector or multiple-sector erase capability
- Sector group protection is user-definable

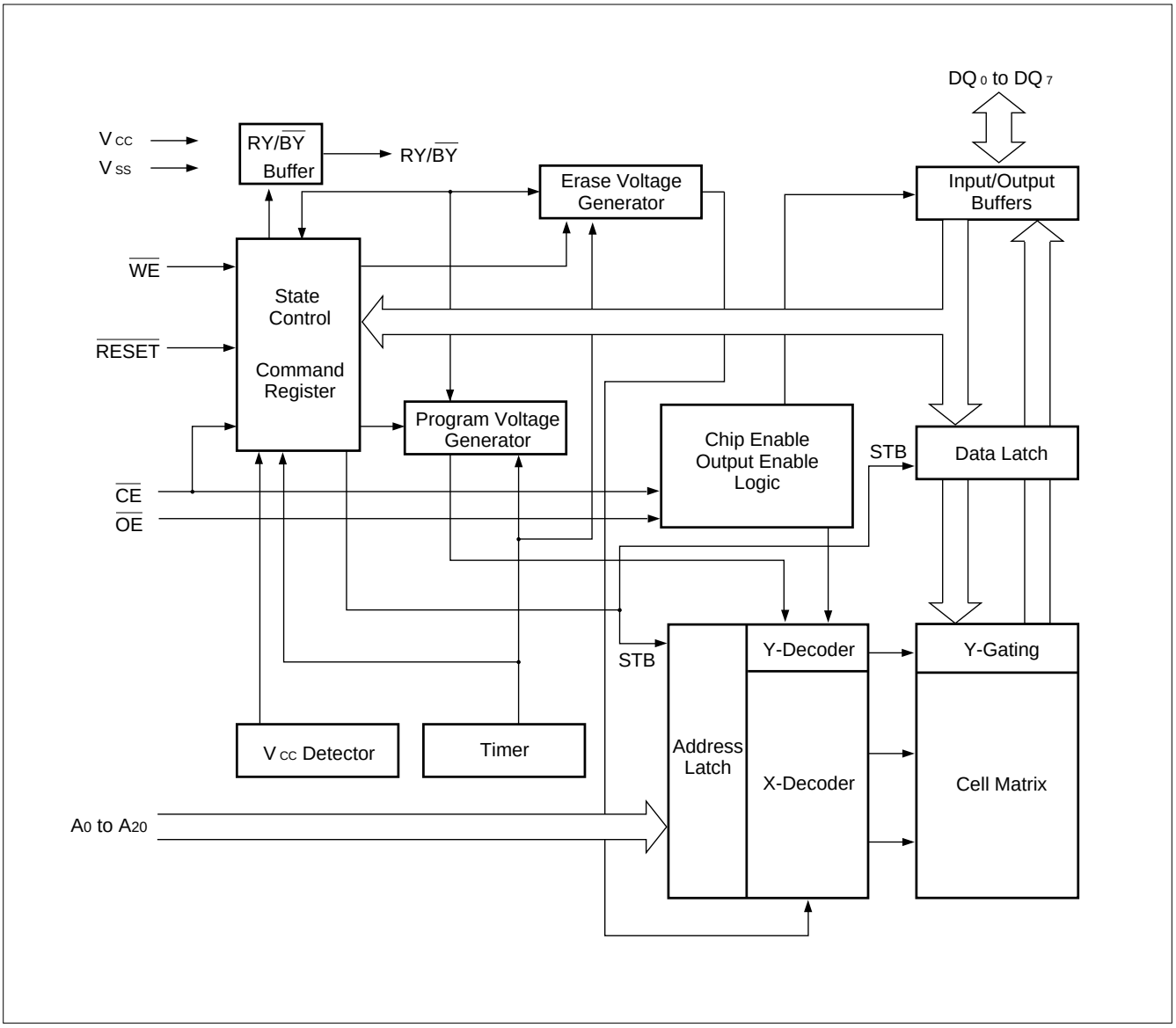


18805B-1

■ PRODUCT SELECTOR GUIDE

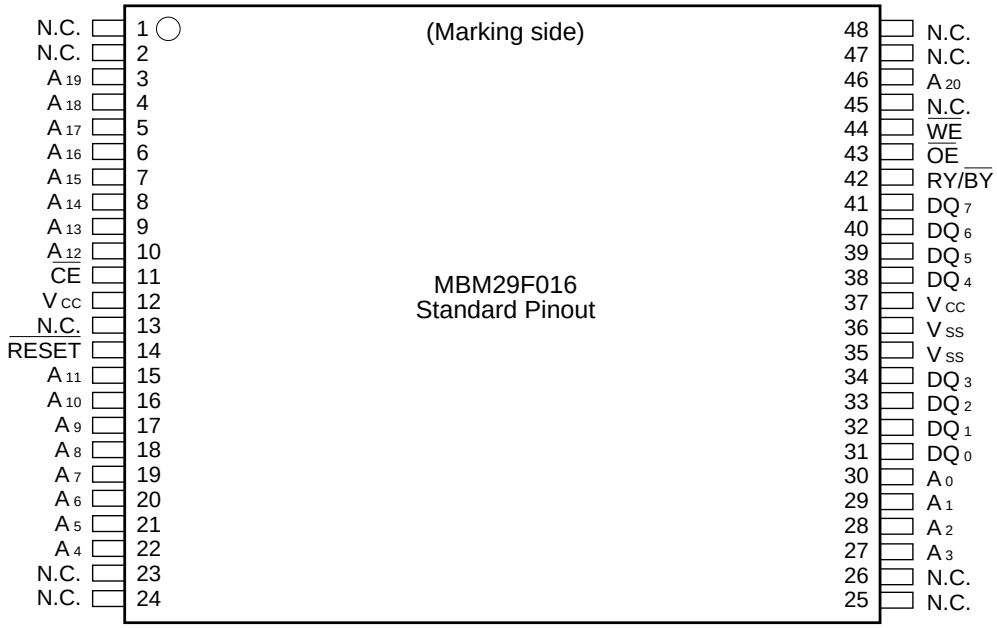
Part No		MBM29F016	
Ordering Part No	V_{CC} = 5.0 V ± 5%	–90	—
	V_{CC} = 5.0 V ± 10%	—	–12
Max Access Time (ns)		90	120
$\overline{CE}$ Access (ns)		90	120
$\overline{OE}$ Access (ns)		40	50

■ BLOCK DIAGRAM



■ CONNECTION DIAGRAMS

TSOP



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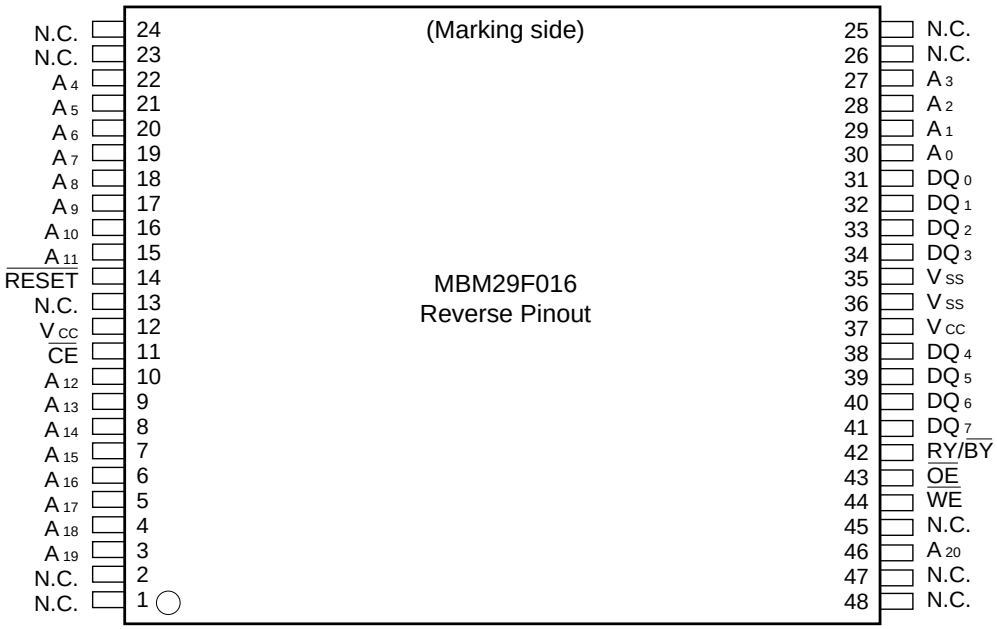


FPT-48P-M20

■ LOGIC SYMBOL

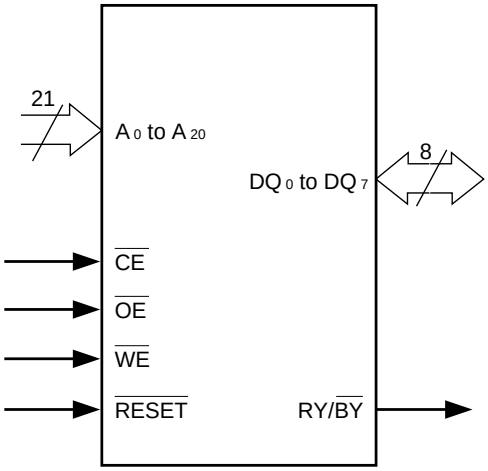


Table 1 MBM29F016 Pin Configuration

Pin	Function
A_0 to A_{20}	Address Inputs
DQ_0 to DQ_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready-Busy Output
$\overline{RESET}$	Hardware Reset Pin/Sector Protection Unlock
NC	No Internal Connection
V_{SS}	Device Ground
V_{CC}	Device Power Supply (5.0 V ± 10 % or ± 5 %)

Table 2 MBM29F016 User Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_6	A_9	DQ_0 to DQ_7	$\overline{RESET}$
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	V_{ID}	Code	H
Auto-Select Device Code (1)	L	L	H	H	L	L	V_{ID}	Code	H
Read (3)	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	High-Z	H
Output Disable	L	H	H	X	X	X	X	High-Z	H
Write	L	H	L	A_0	A_1	A_6	A_9	D_{IN}	H
Enable Sector Group Protection (2)	L	V_{ID}	L	X	X	X	V_{ID}	X	H
Verify Sector Group Protection (2)	L	L	H	L	H	L	V_{ID}	Code	H
Temporary Sector Group Unprotection	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware)	X	X	X	X	X	X	X	High-Z	L

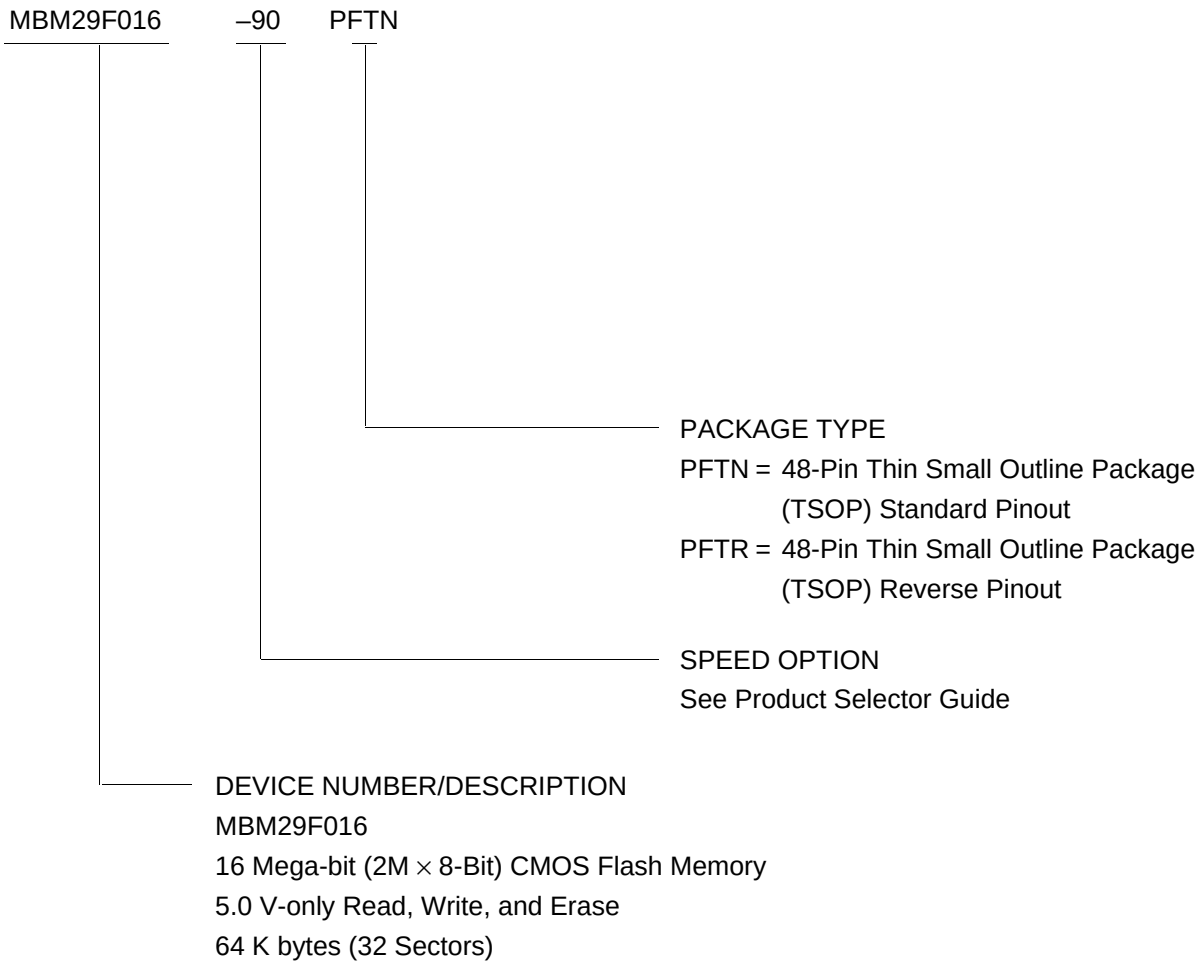
Legend:
L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

Notes:
1. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 6.*
2. *Refer to the section on Sector Group Protection.*
3. $\overline{WE}$ *can be* V_{IL} *if* $\overline{OE}$ *is* V_{IL}, $\overline{OE}$ *at* V_{IH} *initiates the write operations.*

■ ORDERING INFORMATION

Standard Products

Fujitsu standard products are available in several packages. The order number is formed by a combination of:



Read Mode

The MBM29F016 has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}-t_{OE} time).

Standby Mode

There are two ways to implement the standby mode on the MBM29F016 device, one using both the $\overline{CE}$ and $\overline{RESET}$ pins; the other via the $\overline{RESET}$ pin only.

When using both pins, a CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ inputs both held at V_{CC}±0.3 V. Under this condition the current consumed is less than 5 µA. A TTL standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ pins held at V_{IH}. Under this condition the current is reduced to approximately 1 mA. The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the $\overline{RESET}$ pin only, a CMOS standby mode is achieved with $\overline{RESET}$ input held at V_{SS}±0.3 V ($\overline{CE}$ = "H" or "L"). Under this condition the current consumed is less than 5 µA. A TTL standby mode is achieved with $\overline{RESET}$ pin held at V_{IL} ($\overline{CE}$ = "H" or "L"). Under this condition the current required is reduced to approximately 1 mA. Once the $\overline{RESET}$ pin is taken high, the device requires 500 ns of wake up time before outputs are valid for read access.

In the standby mode the outputs are in the high impedance state, independent of the $\overline{OE}$ input.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All addresses are don't cares except A_0, A_1, and A_6. (see Table 3)

The manufacturer and device codes may also be read via the command register, for instances when the MBM29F016 is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in Table 6 (refer to Autoselect Command section).

Byte 0 (A_0 = V_{IL}) represents the manufacturer's code (Fujitsu=04H) and byte 1 (A_0=V_{IH}) the device identifier code for MBM29F016 = ADH. These two bytes are given in the table 3. All identifiers for manufacturer and device will exhibit odd parity with DQ_7 defined as the parity bit. In order to read the proper device codes when executing the Autoselect, A_1 must be V_{IL} (see Table 3).

The Autoselect mode also facilitates the determination of sector group protection in the system. By performing a read operation at the address location XX02H with the higher order address bits A_{18}, A_{19} and A_{20} set to the desired sector group address, the device will return 01H for a protected sector group and 00H for a non-protected sector group.

Table 3 MBM29F016 Sector Protection Verify Autoselect Codes

Type	A_{18} to A_{20}			A_6	A_1	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer's Code	X	X	X	V_{IL}	V_{IL}	V_{IL}	04H	0	0	0	0	0	1	0	0
Device Code	X	X	X	V_{IL}	V_{IL}	V_{IH}	ADH	1	0	1	0	1	1	0	1
Sector Group Protection	Sector Group Addresses			V_{IL}	V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

**Outputs 01H at protected sector addresses and outputs 00H at unprotected sector addresses.*

Table 4 Sector Address Table

	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	Address Range
SA0	0	0	0	0	0	000000h to 00FFFFh
SA1	0	0	0	0	1	010000h to 01FFFFh
SA2	0	0	0	1	0	020000h to 02FFFFh
SA3	0	0	0	1	1	030000h to 03FFFFh
SA4	0	0	1	0	0	040000h to 04FFFFh
SA5	0	0	1	0	1	050000h to 05FFFFh
SA6	0	0	1	1	0	060000h to 06FFFFh
SA7	0	0	1	1	1	070000h to 07FFFFh
SA8	0	1	0	0	0	080000h to 08FFFFh
SA9	0	1	0	0	1	090000h to 09FFFFh
SA10	0	1	0	1	0	0A0000h to 0AFFFFh
SA11	0	1	0	1	1	0B0000h to 0BFFFFh
SA12	0	1	1	0	0	0C0000h to 0CFFFFh
SA13	0	1	1	0	1	0D0000h to 0DFFFFh
SA14	0	1	1	1	0	0E0000h to 0EFFFFh
SA15	0	1	1	1	1	0F0000h to 0FFFFFh
SA16	1	0	0	0	0	100000h to 10FFFFh
SA17	1	0	0	0	1	110000h to 11FFFFh
SA18	1	0	0	1	0	120000h to 12FFFFh
SA19	1	0	0	1	1	130000h to 13FFFFh
SA20	1	0	1	0	0	140000h to 14FFFFh
SA21	1	0	1	0	1	150000h to 15FFFFh
SA22	1	0	1	1	0	160000h to 16FFFFh
SA23	1	0	1	1	1	170000h to 17FFFFh
SA24	1	1	0	0	0	180000h to 18FFFFh
SA25	1	1	0	0	1	190000h to 19FFFFh
SA26	1	1	0	1	0	1A0000h to 1AFFFFh
SA27	1	1	0	1	1	1B0000h to 1BFFFFh
SA28	1	1	1	0	0	1C0000h to 1CFFFFh
SA29	1	1	1	0	1	1D0000h to 1DFFFFh
SA30	1	1	1	1	0	1E0000h to 1EFFFFh
SA31	1	1	1	1	1	1F0000h to 1FFFFFh

Table 5 Sector Group Addresses

	A_{20}	A_{19}	A_{18}	Sectors
SGA0	0	0	0	SA0 to SA3
SGA1	0	0	1	SA4 to SA7
SGA2	0	1	0	SA8 to SA11
SGA3	0	1	1	SA12 to SA15
SGA4	1	0	0	SA16 to SA19
SGA5	1	0	1	SA20 to SA23
SGA6	1	1	0	SA24 to SA27
SGA7	1	1	1	SA28 to SA31

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Group Protection

The MBM29F016 features hardware sector group protection. This feature will disable both program and erase operations in any combination of eight sector groups of memory. Each sector group consists of four adjacent sectors grouped in the following pattern: sectors 0-3, 4-7, 8-11, 12-15, 16-19, 20-23, 24-27, and 28-31 (see Table 5). The sector group protection feature is enabled using programming equipment at the user's site. The device is shipped with all sector groups unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, (suggest V_{ID} = 11.5 V), $\overline{CE}$ = V_{IL}. The sector addresses (A_{20}, A_{19}, and A_{18}) should be set to the sector to be protected. Tables 4 and 5 define the sector address for each of the thirty two (32) individual sectors, and the sector group address for each of the eight (8) individual group sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. Refer to figures 14 and 21 for sector protection waveforms and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{20}, A_{19}, and A_{18}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical “1” code at device output DQ_0 for a protected sector. Otherwise the device will produce 00H for unprotected sector. In this mode, the lower order addresses, except for A_0, A_1, and A_6 are don’t care. Address locations with A_1 = V_{IL} are reserved for Autoselect manufacturer and device codes.

It is also possible to determine if a sector group is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A_{20}, A_{19}, and A_{18}) are the desired sector group address will produce a logical “1” at DQ_0 for a protected sector group. See Table 3 for Autoselect codes.

Temporary Sector Group Unprotection

This feature allows temporary unprotection of previously protected sector groups of the MBM29F016 device in order to change data. The Sector Group Unprotection mode is activated by setting the $\overline{RESET}$ pin to high voltage (12 V). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the 12 V is taken away from the $\overline{RESET}$ pin, all the previously protected sector groups will be protected again. Refer to Figures 13 and 20.

Table 6 MBM29F016 Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset*	1	XXXH	F0H										
Reset/Read*	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD				
Autoselect	3	555H	AAH	2AAH	55H	555H	90H						
Byte Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (H or L), Data (B0H)											
Sector Erase Resume		Erase can be resumed after suspend with Addr (H or L), Data (30H)											

Notes:
1. *Address bits A_{11} to A_{20} = X = H or L for all address commands except or Program Address (PA) and Sector Address (SA).*
2. *Bus operations are defined in Table 2.*
3. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A_{20}, A_{19}, A_{18}, A_{17}, and A_{16} will uniquely select any sector.
4. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data is latched on the falling edge of $\overline{WE}$.
5. *Read and Byte program functions to non-erasing sectors are allowed in the Erase Suspend mode.*
6. *The system should generate the following address patterns: 555H or 2AAH to addresses A_0 to A_{10}*

∗ *Either of the two reset commands will reset the device.*

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 6 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Moreover, both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desirable system design practice.

The device contains an autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of 04H. A read cycle from address XX01H returns the device code ADH (see Table 3).

All manufacturer and device codes will exhibit odd parity with the DQ_7 defined as the parity bit.

Sector state (protection or unprotection) will be informed by address XX02H.

Scanning the sector group addresses (A_{18}, A_{19}, A_{20}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" at device output DQ_0 for a protected sector group.

To terminate the operation, it is necessary to write the read/reset command sequence into the register and also to write the autoselect command during the operation, execute it after writing read/reset command sequence.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program™ Algorithm command sequence, the system is *not* required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

This automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which time the device returns to the read mode and addresses are no longer latched. (see Table 7, Hardware Sequence Flags) Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. $\overline{Data}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored. If a hardware reset occurs during the programming operation, it is impossible to guarantee the data are being written.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 15 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase™ Algorithm command sequence the device will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ_7 is "1" (see Write Operation Status section) at which time the device returns to read the mode.

Figure 16 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector

address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (Data = 30H) is latched on the rising edge of $\overline{WE}$. After time-out of 50 µs from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on Table 6. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 50 µs otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 50 µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 50 µs time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the device to the read mode, ignoring the previous command string. Resetting the device once execution has begun will corrupt the data in that sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for DQ_3, Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 31).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 50 µs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ_7 is “1” (see Write Operation Status section) at which time the device returns to the read mode. $\overline{Data}$ polling must be performed at an address within any of the sectors being erased.

Figure 16 illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Erase Suspend

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program™ Algorithm. Writting the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Any other command written during the Erase Suspend mode will be ignored except the Erase Resume command. Writing the Erase Resume command resumes the erase operation. The addresses are “don't-cares” when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 15 µs to suspend the erase operation. When the device has entered the erase-suspended mode, the $RY/\overline{BY}$ output pin and the DQ_7 bit will be at logic “1”, and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. (See the section on DQ_2).

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Byte Program. This program mode is known as the erase-suspend-program mode. Again, program-

ming in this mode is the same as programming in the regular Byte Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended program operation is detected by the $RY/\overline{BY}$ output pin, $\overline{Data}$ polling of DQ_7, or by the Toggle Bit I (DQ_6) which is the same as the regular Byte Program operation. Note that DQ_7 must be read from the byte program address while DQ_6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Write Operation Status

Table 7 Hardware Sequence Flags

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program™ Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded Erase™ Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	1	Toggle (Note 1)
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle (Note 2)	0	1	1 (Note 3)
Exceeded Time Limits	Embedded Program™ Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded Erase™ Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	1	N/A

Notes:

1. *Performing successive read operations from the erase-suspended sector will cause DQ_2 to toggle.*
2. *Performing successive read operations from any address will cause DQ_6 to toggle.*
3. *Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the DQ_2 bit. However, successive reads from the erase-suspended sector will cause DQ_2 to toggle.*

DQ_7

$\overline{Data}$ Polling

The MBM29F016 device features $\overline{Data}$ Polling as a method to indicate to the host that the embedded algorithms are in progress or completed. During the Embedded Program™ Algorithm, an attempt to read the device will produce the complement of the data last written to DQ_7. Upon completion of the Embedded Program™ Algorithm, an attempt to read the device will produce the true data last written to DQ_7. During the Embedded Erase™ Algorithm, an attempt to read the device will produce a "0" at the DQ_7 output. Upon completion of the Embedded Erase™ Algorithm an attempt to read the device will produce a "1" at the DQ_7 output. The flowchart for $\overline{Data}$ Polling (DQ_7) is shown in Figure 17.

$\overline{Data}$ polling will also flag the entry into Erase Suspend. DQ_7 will switch "0" to "1" at the start of the Erase Suspend

mode. Please note that the address of an erasing sector must be applied in order to observe DQ_7 in the Erase Suspend Mode.

During Program in Erase Suspend, $\overline{\text{Data}}$ polling will perform the same as in regular program execution outside of the suspend mode.

For chip erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, the $\overline{\text{Data}}$ Polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. $\overline{\text{Data}}$ Polling must be performed at sector address within any of the sectors being erased and not a sector that is within a protected sector group. Otherwise, the status may not be valid.

Just prior to the completion of Embedded Algorithm operation DQ_7 may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the device is driving status information on DQ_7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DQ_7 has a valid data, the data outputs on DQ_0 to DQ_6 may be still invalid. The valid data on DQ_0 to DQ_7 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, Erase Suspend, erase-suspend-program mode, or sector erase time-out (see Table 7).

See Figure 8 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ_6

Toggle Bit I

The MBM29F016 also features the “Toggle Bit I” as a method to indicate to the host system that the embedded algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the device *at any address* will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on *the next* successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit I is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For Sector Erase, the Toggle Bit I is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. The Toggle Bit I is active during the sector erase time out.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ_6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ_6 to toggle. See Figure 9 for the Toggle Bit I timing specifications and diagrams.

DQ_5

Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ_5 will produce a “1”. This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Table 2.

The DQ_5 failure condition may also appear if a user tries to program a 1 to a location that is previously programmed to 0. In this case the device locks out and never completes the Embedded Program™ Algorithm. Hence, the system never reads a valid data on DQ_7 bit and DQ_6 never stops toggling. Once the device has exceeded timing limits, the DQ_5 bit will indicate a “1.” Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset the device.

DQ_3

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ_3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit I are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DQ_3 may be used to determine if the sector erase timer window is still open. If DQ_3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands (other than Erase Suspend) to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit I. If DQ_3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent sector erase command. If DQ_3 were high on the second status check, the command may not have been accepted.

Refer to Table 7: Hardware Sequence Flags

DQ_2

Toggle Bit II

This toggle bit, along with DQ_6, can be used to determine whether the device is in the Embedded Erase™ Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase™ Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the device is in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic "1" at the DQ_2 bit.

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	toggles	1
Erase	0	toggles	toggles
Erase Suspend Read (1) (Erase-Suspended Sector)	1	1	toggles
Erase Suspend Program	$\overline{DQ_7}$ (2)	toggles	1 (2)

Notes:

1. *These status flags apply when outputs are read from a sector that has been erase-suspended.*
2. *These status flags apply when outputs are read from the byte address of the non-erase suspended sector.*

DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ_7, is summarized as follows:

For example, DQ_2 and DQ_6 can be used together to determine the erase-suspend-read mode (DQ_2 toggles while DQ_6 does not). See also Table 7 and Figure 14.

Furthermore, DQ_2 can also be used to determine which sector is being erased. When the device is in the erase mode, DQ_2 toggles if this bit is read from the erasing sector.

RY/$\overline{BY}$

Ready/Busy

The MBM29F016 provides a RY/ $\overline{BY}$ open-drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or has been completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. When the RY/ $\overline{BY}$ pin is low, the device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If the MBM29F016 is placed in an Erase Suspend mode, the RY/$\overline{BY}$ output will be high, by means of connecting with a pull-up resistor to V_{CC}.

During programming, the RY/$\overline{BY}$ pin is driven low after the rising edge of the fourth $\overline{WE}$ pulse. During an erase operation, the RY/$\overline{BY}$ pin is driven low after the rising edge of the sixth $\overline{WE}$ pulse. The RY/$\overline{BY}$ pin will indicate a busy condition during $\overline{RESET}$ pulse. Refer to Figure 10 for a detailed timing diagram. The RY/ $\overline{BY}$ pin is pulled high in standby mode.

Since this is an open-drain output, several RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to V_{CC}.

$\overline{RESET}$

Hardware Reset

The MBM29F016 device may be reset by driving the $\overline{RESET}$ pin to V_{IL}. The $\overline{RESET}$ pin must be kept low (V_{IL}) for at least 500 ns. Any operation in progress will be terminated and the internal state machine will be reset to the read mode 20 µs after the $\overline{RESET}$ pin is driven low. If a hardware reset occurs during a program operation, the data at that particular location will be indeterminate.

When the $\overline{RESET}$ pin is low and the internal reset is complete, the device goes to standby mode and cannot be accessed. Also, note that all the data output pins are tri-stated for the duration of the $\overline{RESET}$ pulse. Once the $\overline{RESET}$ pin is taken high, the device requires 500 ns of wake up time until outputs are valid for read access.

The $\overline{RESET}$ pin may be tied to the system reset input. Therefore, if a system reset occurs during the Embedded Program or Erase Algorithm, the device will be automatically reset to read mode and this will enable the system's microprocessor to read the boot-up firmware from the Flash memory.

Data Protection

The MBM29F016 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completions of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE}$ = $\overline{CE}$ =V_{IL} and $\overline{OE}$ = V_{IH} will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –45°C to +125°C
Ambient Temperature with Power Applied ..... –25°C to +85°C
Voltage with Respect to Ground All pins except A_9, $\overline{OE}$, $\overline{RESET}$ (Note 1) ..... –2.0 V to +7.0 V
V_{CC} (Note 1) ..... –2.0 V to +7.0 V
A_9, $\overline{OE}$, $\overline{RESET}$ (Note 2) ..... –2.0 V to +13.5 V

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} +0.5 V. During voltage transitions, outputs may positive overshoot to V_{CC} +2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A_9, $\overline{OE}$, $\overline{RESET}$ pins are –0.5 V. During voltage transitions, A_9, $\overline{OE}$, $\overline{RESET}$ pins may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9, $\overline{OE}$, $\overline{RESET}$ are +13.0 V which may overshoot to 13.5 V for periods up to 20 ns.*

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

■ OPERATING RANGES

Commercial Devices

Ambient Temperature (T_A) ..... 0°C to +70°C

V_{CC} Supply Voltages

V_{CC} for MBM29F016-90 ..... +4.75 V to +5.25 V
V_{CC} for MBM29F016-12 ..... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

■ MAXIMUM OVERSHOOT

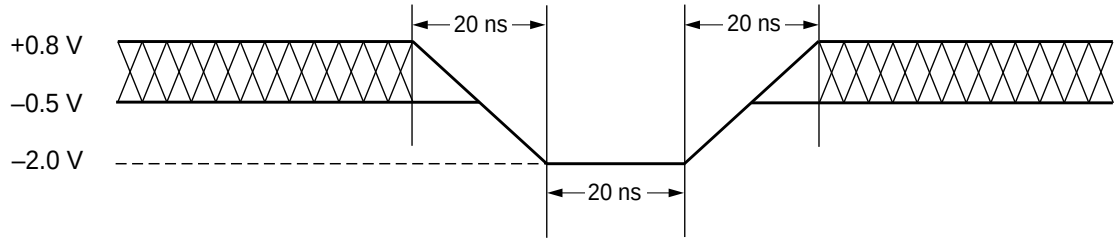


Figure 1 Maximum Negative Overshoot Waveform

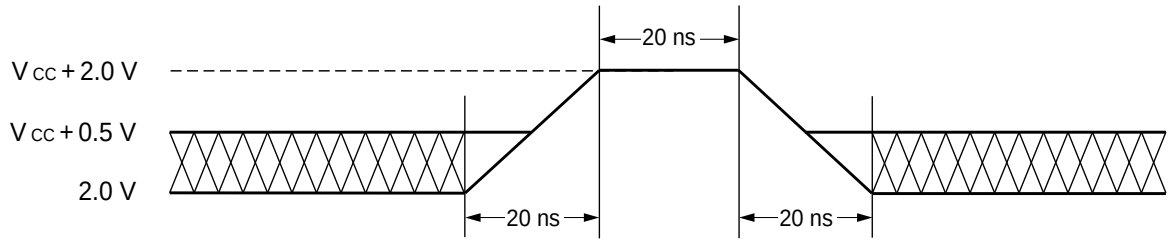


Figure 2 Maximum Positive Overshoot Waveform

■ DC CHARACTERISTICS

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.	—	±1.0	µA
I_{LO}	Outputs Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.	—	±1.0	µA
I_{LIT}	A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	V_{CC} = V_{CC} Max. A_9 , $\overline{OE}$, $\overline{RESET}$= 12.0V	—	50	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	—	40	mA
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	—	60	mA
I_{CC3}	V_{CC} Current (Standby)	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IH}, $\overline{RESET}$ = V_{IH}	—	1.0	mA
I_{CC4}	V_{CC} Current (Standby, Reset)	V_{CC} = V_{CC} Max., $\overline{RESET}$ = V_{IL}	—	1.0	mA
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC}+0.5	V
V_{ID}	Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$, $\overline{RESET}$)	V_{CC} = 5.0V	11.5	12.5	V
V_{OL}	Output Low Voltage Level	I_{OL} = 12mA, V_{CC} = V_{CC} Min.	—	0.45	V
V_{OH}	Output High Voltage Level	I_{OH} = –2.5mA, V_{CC} = V_{CC} Min.	2.4	—	V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2	4.2	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is 2 mA/MHz, with $\overline{OE}$ V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*

CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.	—	±1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max.	—	±1.0	µA
I_{LIT}	A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	V_{CC} = V_{CC} Max. A_9, $\overline{OE}$, $\overline{RESET}$= 12.0V	—	50	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	—	40	mA
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	—	60	mA
I_{CC3}	V_{CC} Current (Standby)	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{CC} ±0.3V, $\overline{RESET}$ = V_{CC} ±0.3V	—	5	µA
I_{CC4}	V_{CC} Current (Standby, Reset)	V_{CC} = V_{CC} Max., $\overline{RESET}$ = V_{SS} ±0.3V	—	5	µA
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		0.7xV_{CC}	V_{CC}+0.3	V
V_{ID}	Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$, $\overline{RESET}$)	V_{CC} = 5.0V	11.5	12.5	V
V_{OL}	Output Low Voltage Level	I_{OL} = 12.0 mA, V_{CC} = V_{CC} Min.	—	0.45	V
V_{OH1}	Output High Voltage Level	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85xV_{CC}	—	V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC}–0.4	—	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2	4.2	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*

■ AC CHARACTERISTICS

Read only Operations Characteristics

Parameter Symbols		Description	Test Setup		–90 (Note)	–12 (Note)	Unit
JEDEC	Standard						
t_{AVAV}	t_{RC}	Read Cycle Time		Min.	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{IL}	Max.	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Max.	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max.	40	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z		Max.	20	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z		Max.	20	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min.	0	0	ns
	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode		Max.	20	20	µs

Note:

Test Conditions:
Output Load: 1 TTL gate and 100 pF
Input rise and fall times: 20 ns
Input pulse levels: 0.45V to 2.4V
Timing measurement reference level
Input: 0.8 and 2.0V
Output: 0.8 and 2.0V

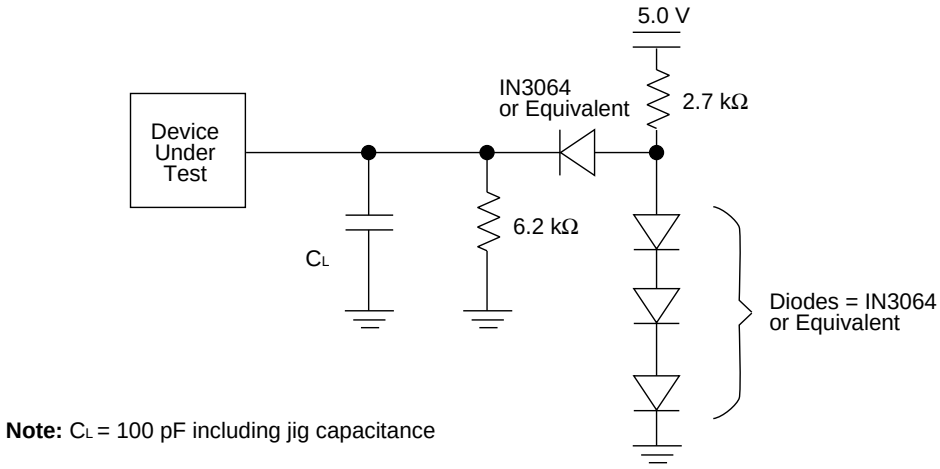


Figure 3 Test Conditions

• Write/Erase/Program Operations

Alternate $\overline{WE}$ Controlled Writes

Parameter Symbols		Description			–90	–12	Unit
JEDEC	Standard						
t_{AVAV}	t_{WC}	Write Cycle Time		Min.	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min.	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min.	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min.	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min.	0	0	ns
	t_{OES}	Output Enable Setup Time		Min.	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read	Min.	0	0	ns
			Toggle Bit I and $\overline{Data}$ Polling	Min.	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min.	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time		Min.	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min.	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min.	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min.	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ.	8	8	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ.	1	1	sec
				Max.	15	15	sec
	t_{VCS}	V_{CC} Setup Time		Min.	50	50	µs
	t_{VLHT}	Voltage Transition Time (Note 2)		Min.	4	4	µs
	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Note 2)		Min.	4	4	µs
	t_{CSP}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active (Note 2)		Min.	4	4	µs
	t_{RP}	$\overline{RESET}$ Pulse Width		Min.	500	500	ns
	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay		Min.	40	50	ns

Notes:

1. This does not include the preprogramming time.

2. This timing is for Sector Protection operation.

■ AC/CHARACTERISTICS

• Write/Erase/Program Operations

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols		Description			–90	–12	Unit
JEDEC	Standard						
t_{AVAV}	t_{WC}	Write Cycle Time		Min.	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min.	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min.	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min.	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min.	0	0	ns
	t_{OES}	Output Enable Setup Time		Min.	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read	Min.	0	0	ns
			Toggle Bit I and $\overline{Data}$ Polling	Min.	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min.	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min.	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min.	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width		Min.	45	50	ns
t_{EHEL}	t_{CPH}	Write Pulse Width High		Min.	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ.	8	8	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note)		Typ.	1	1	sec
				Max.	15	15	sec
	t_{VCS}	V_{CC} Setup Time		Min.	50	50	µs

Note:

This does not include the preprogramming time.

■ SWITCHING WAVEFORMS

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	H or L Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

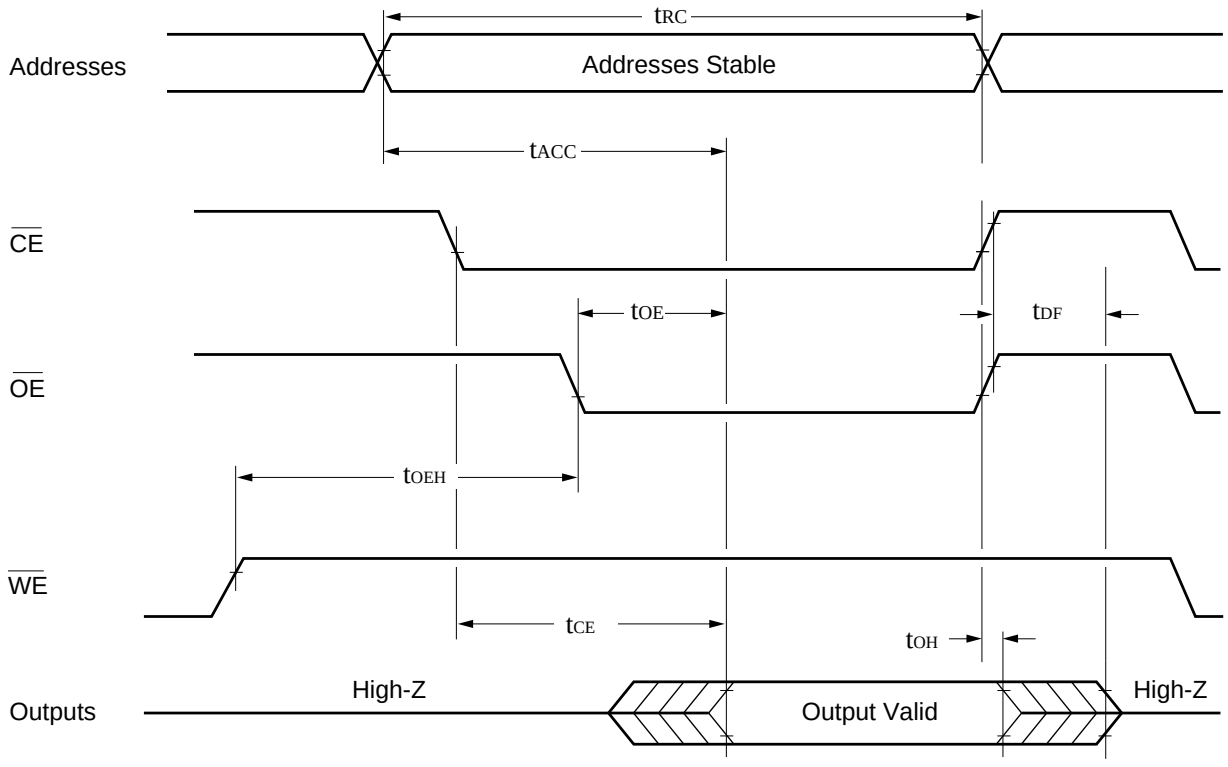
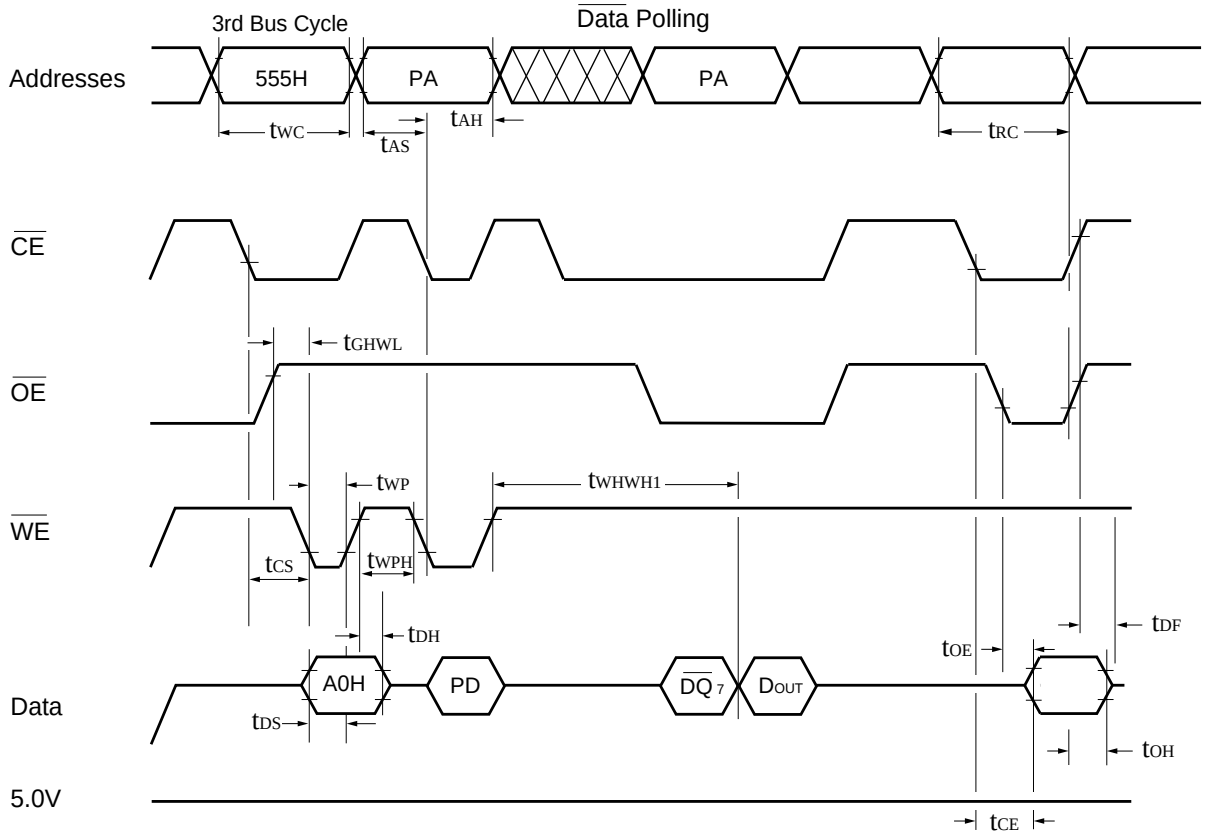


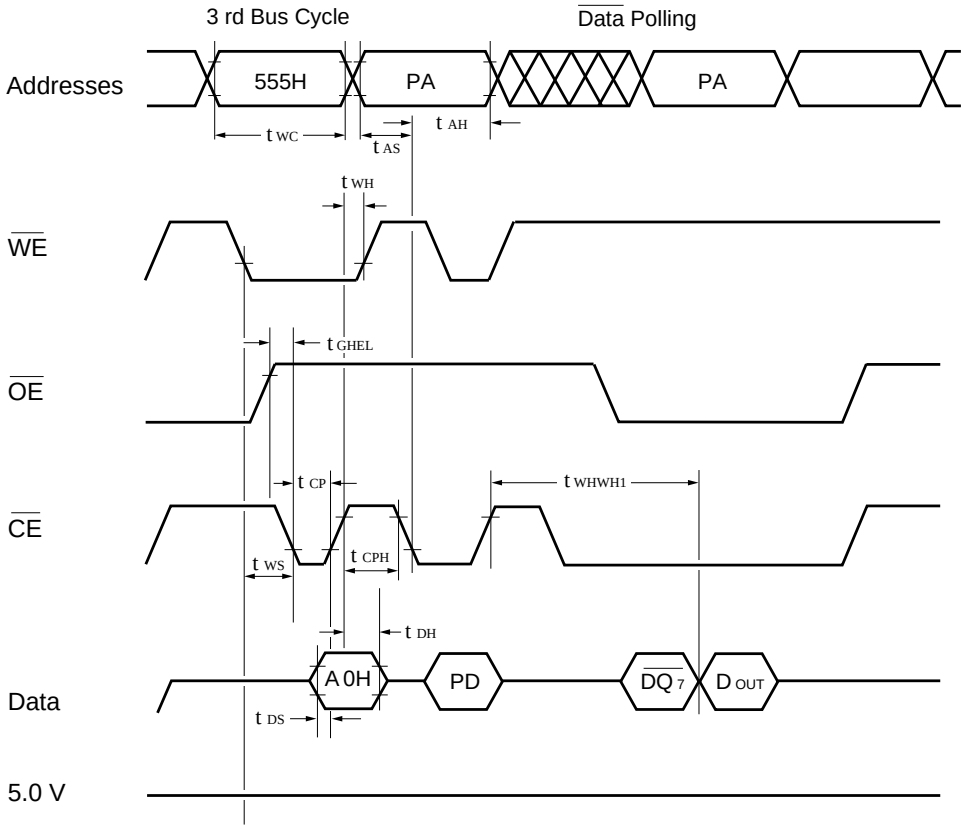
Figure 4 AC Waveforms for Read Operations



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ}_7$ is the output of the complement of the data written to the device.*
4. *D_{OUT} is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

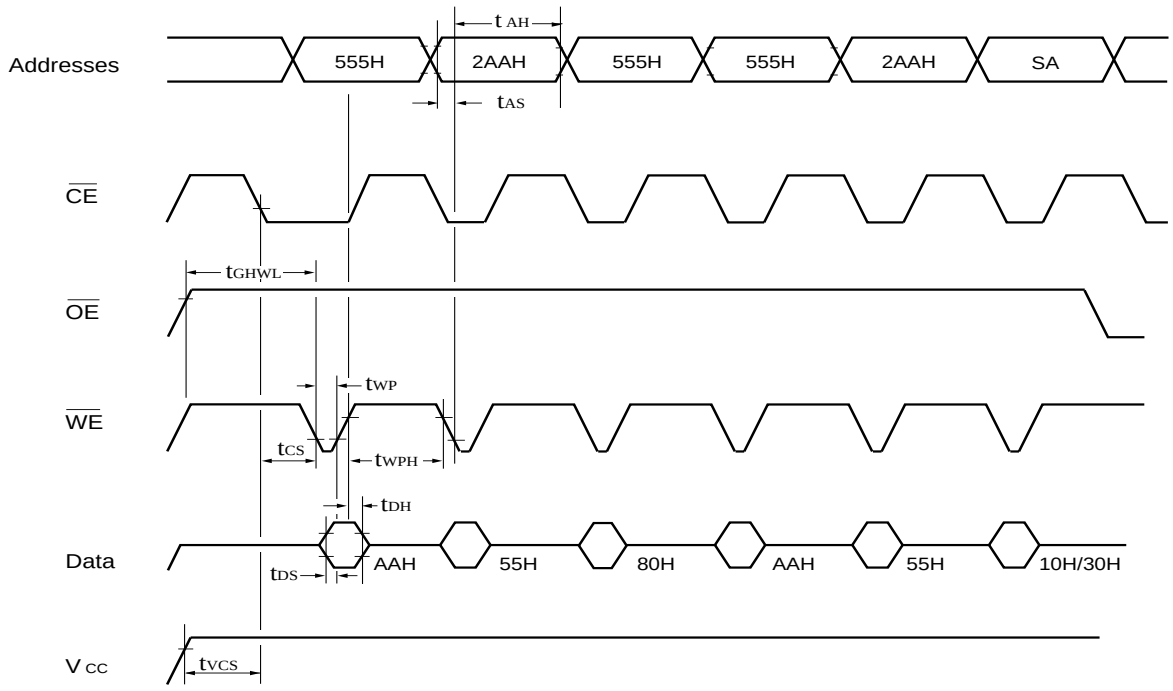
Figure 5 Alternate $\overline{WE}$ Controlled Program Operation Timings



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *DQ_7 is the output of the complement of the data written to the device.*
4. *D_{OUT} is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

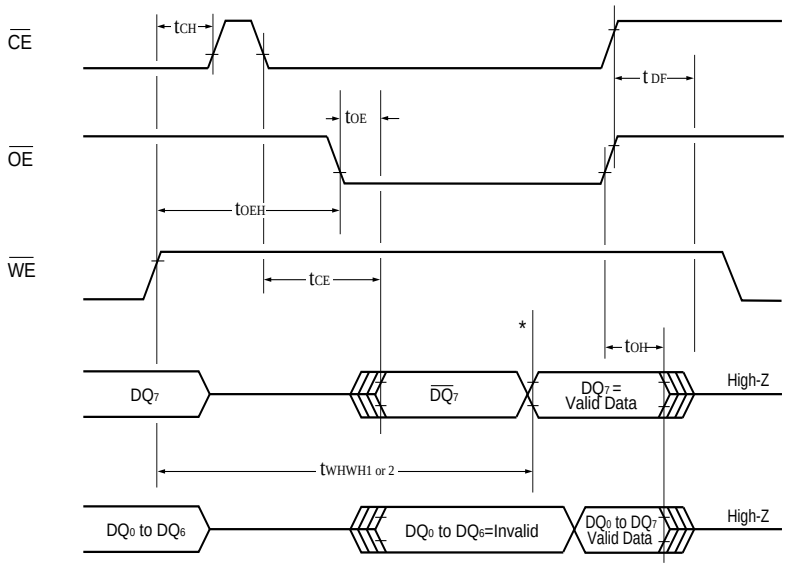
Figure 6 Alternate CE Controlled Program Operation Timings



Note:

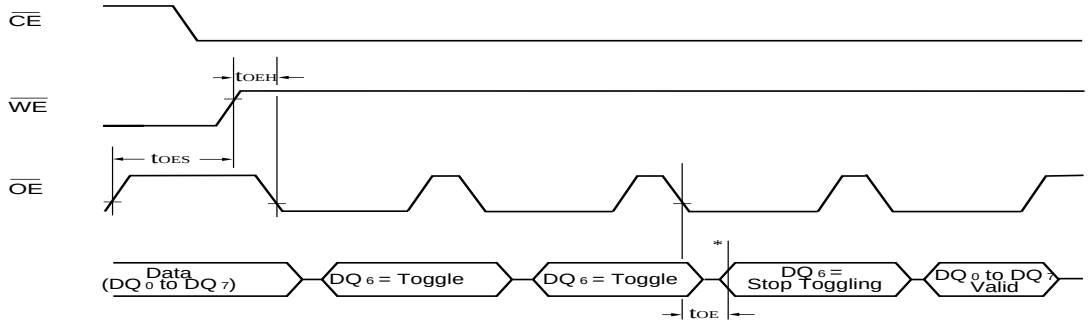
SA is the sector address for Sector Erase. Addresses = 555H for Chip Erase.

Figure 7 AC Waveforms Chip/Sector Erase Operations



*DQ_7 = Valid Data (The device has completed the Embedded operation).

Figure 8 AC Waveforms for $\overline{\text{Data}}$ Polling During Embedded Algorithm Operations



*DQ_6 stops toggling (The device has completed the Embedded operation).

Figure 9 AC Waveforms for Toggle Bit I During Embedded Algorithm Operations

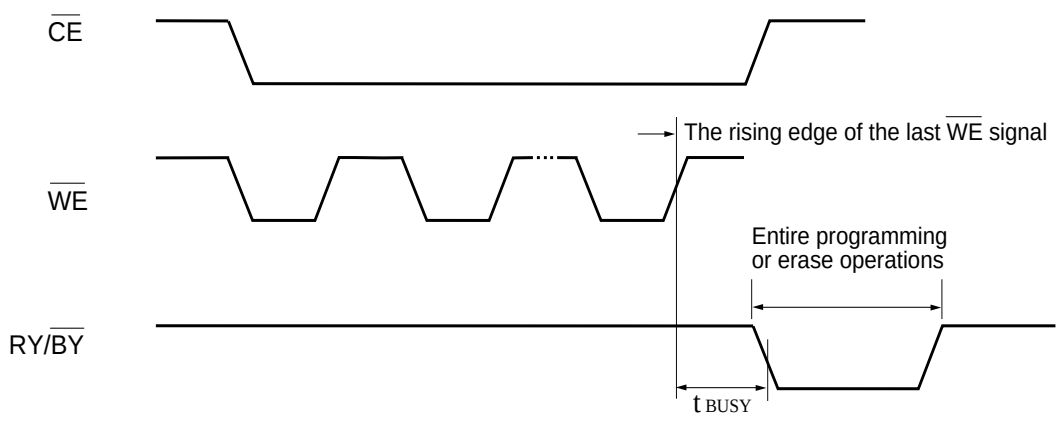


Figure 10 RY/BY Timing Diagram During Program/Erase Operations

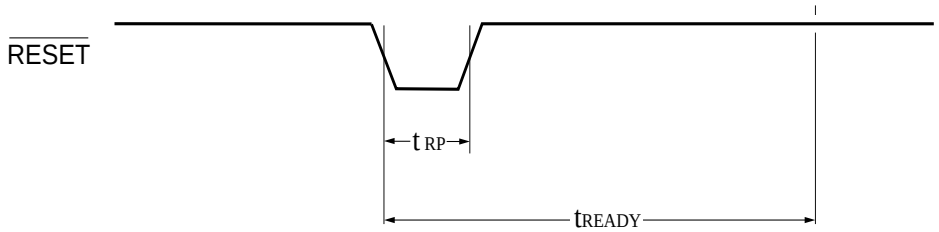
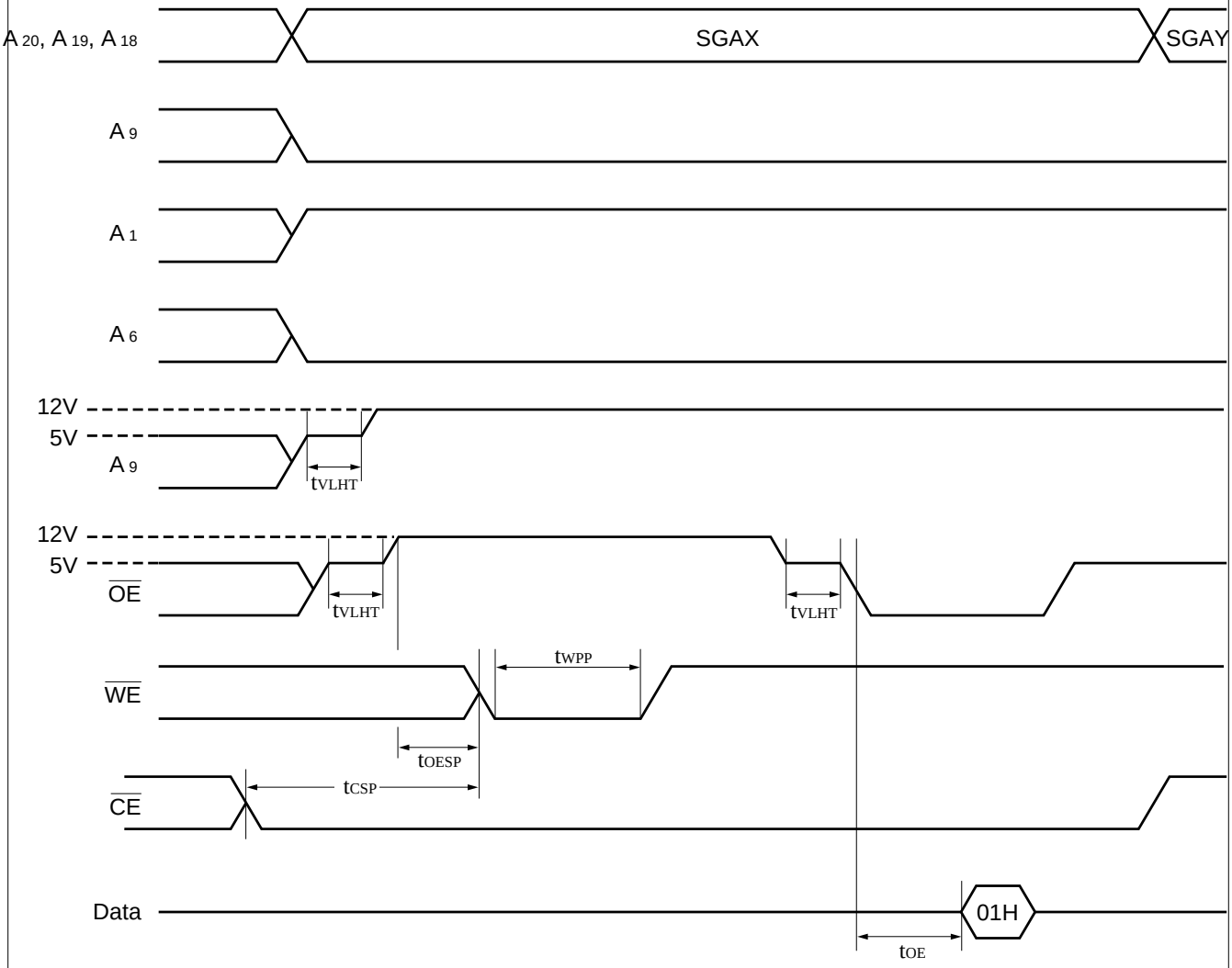


Figure 11 RESET Timing Diagram



SGAX: Sector Group Address for initial sector
SGAY: Sector Group Address for next sector

Figure 12 AC Waveforms for Sector Group Protection

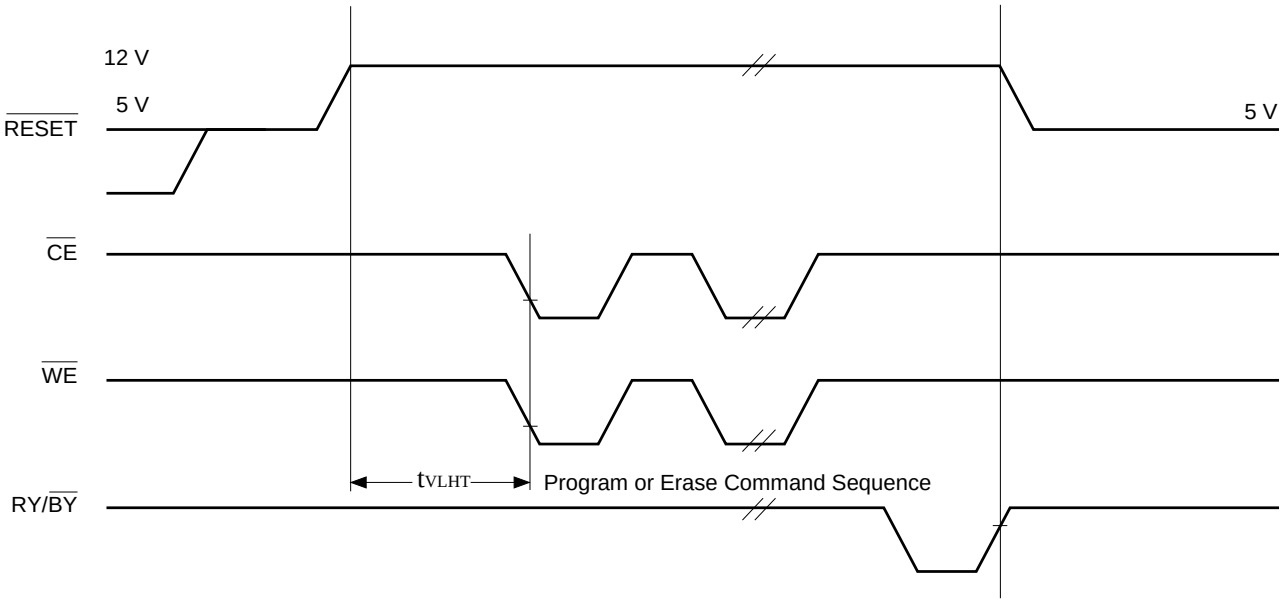
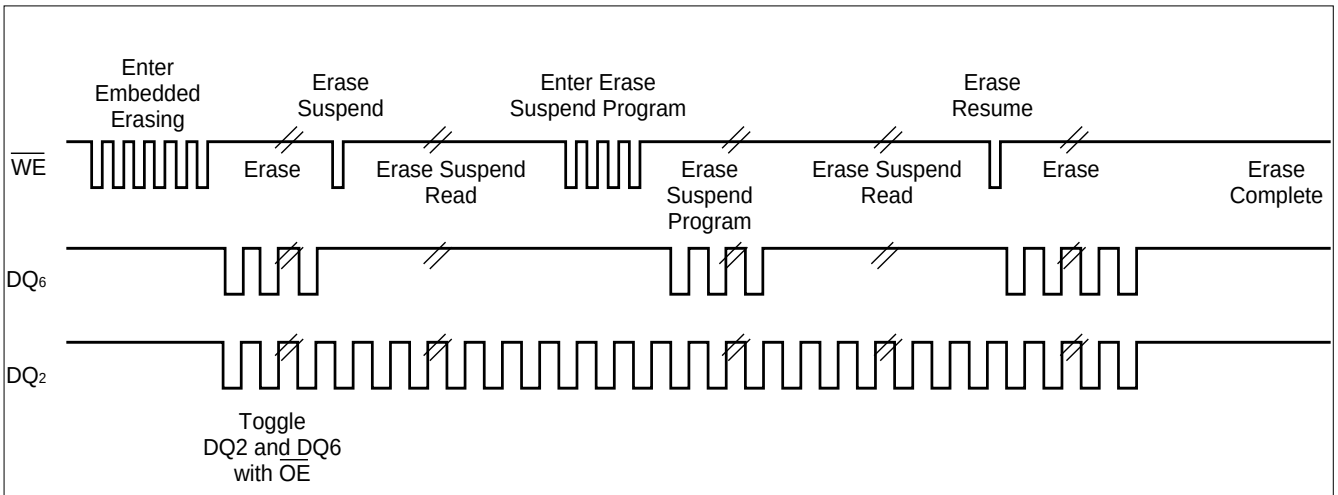


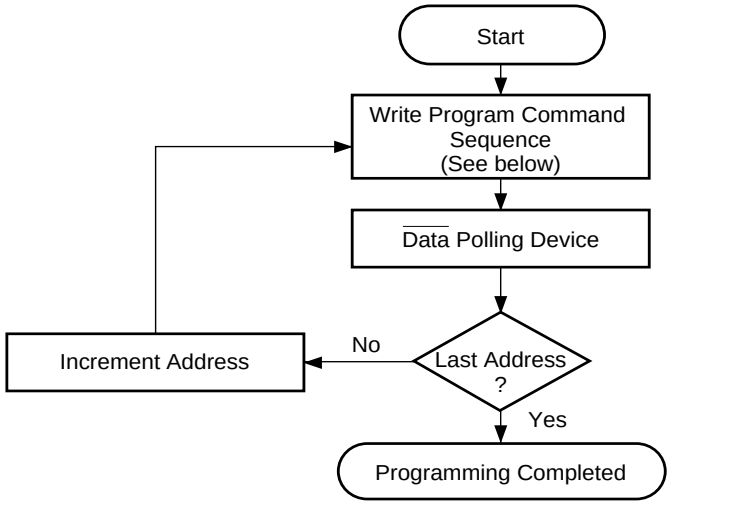
Figure 13 Temporary Sector Group Unprotection



Note:
DQ_2 is read from the erase-suspended sector.

Figure 14 DQ_2 vs. DQ_6

■ EMBEDDED ALGORITHMS



Program Command Sequence (Address/Command):

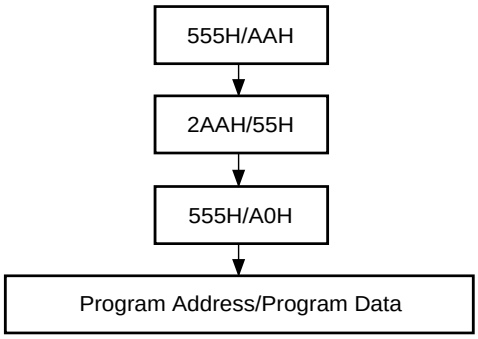
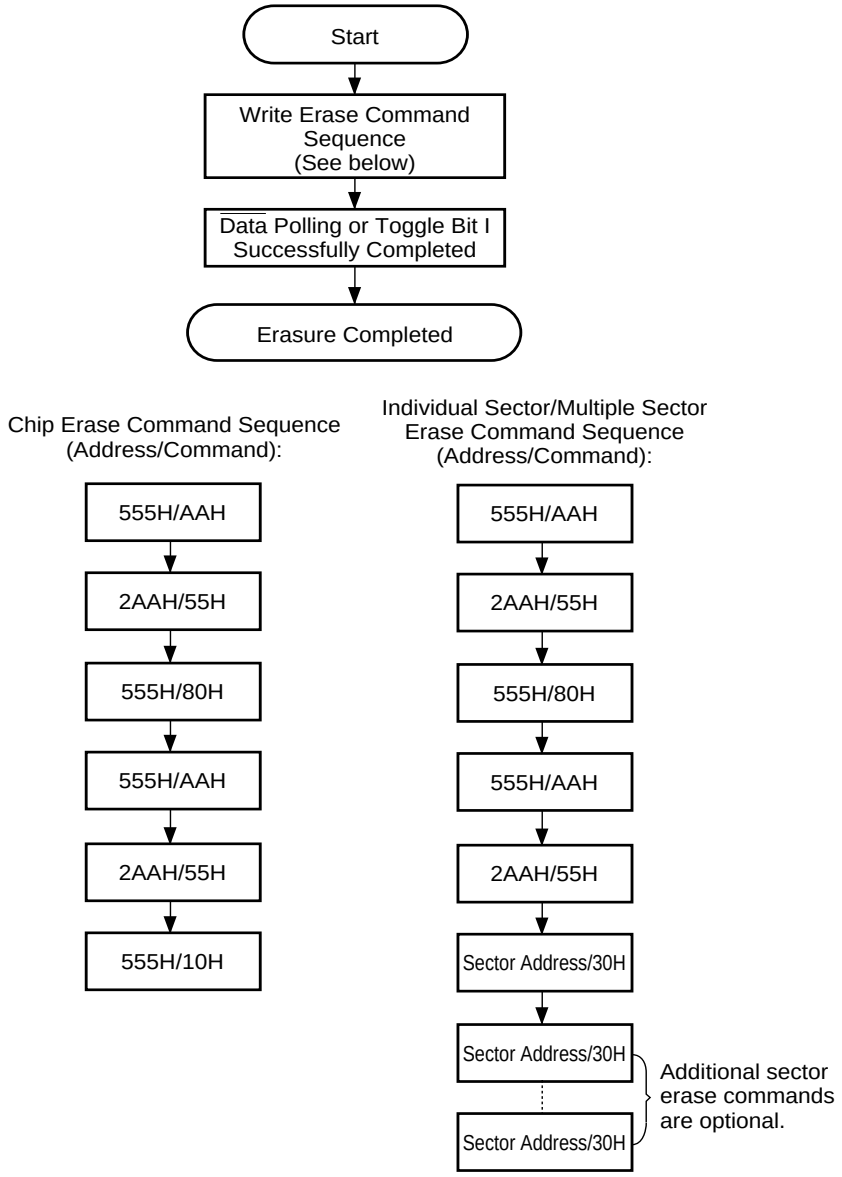


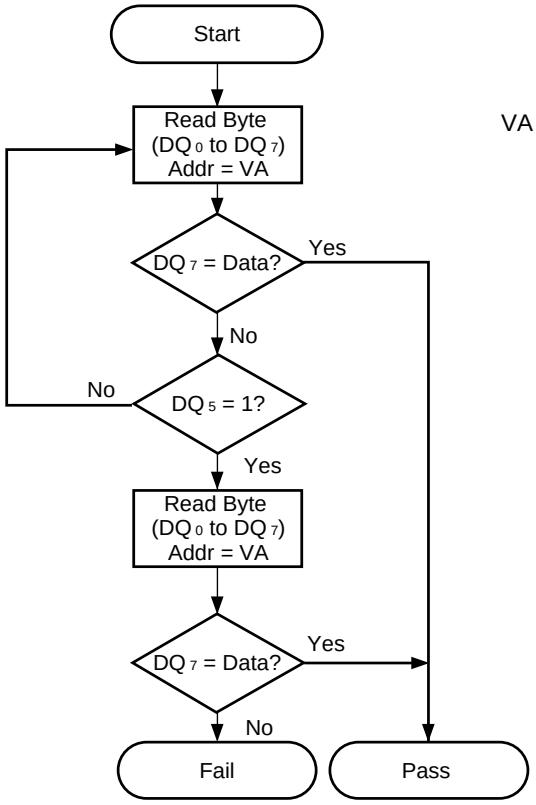
Figure 15 Embedded Programming Algorithm

■ EMBEDDED ALGORITHMS



Note: *To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent sector erase command. If DQ_3 were high on the second status check, the command may not have been accepted.*

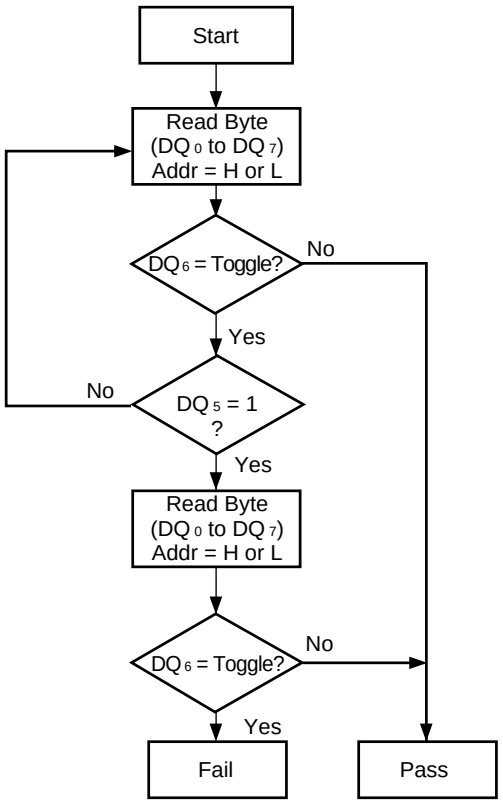
Figure 16 Embedded Erase™ Algorithm



VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase operation
= Any of the sector group address within the sector not being protected during chip erase operation.

Note: *DQ_7 is rechecked even if DQ_5 = "1" because DQ_7 may change simultaneously with DQ_5.*

Figure 17 $\overline{\text{Data}}$ Polling Algorithm



Note: *DQ_6 is rechecked even if DQ_5 = "1" because DQ_6 may stop toggling at the same time as DQ_5 changing to "1" .*

Figure 18 Toggle Bit I Algorithm

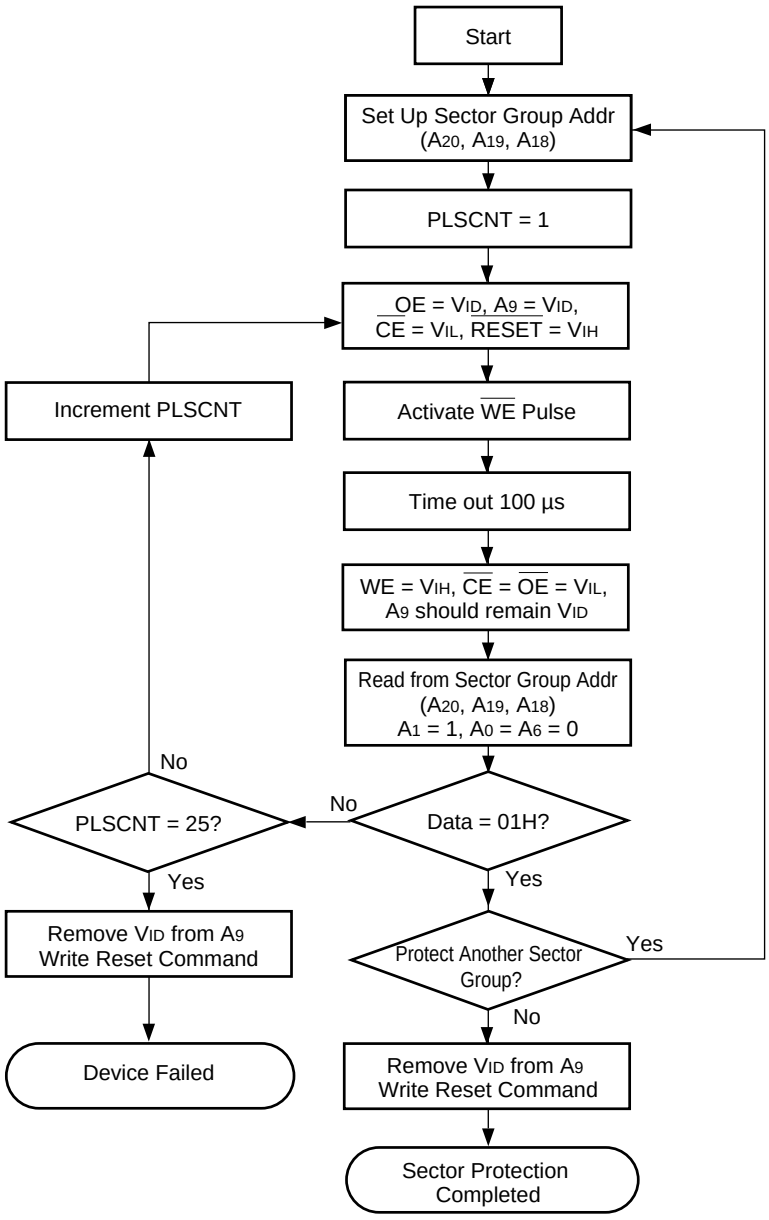
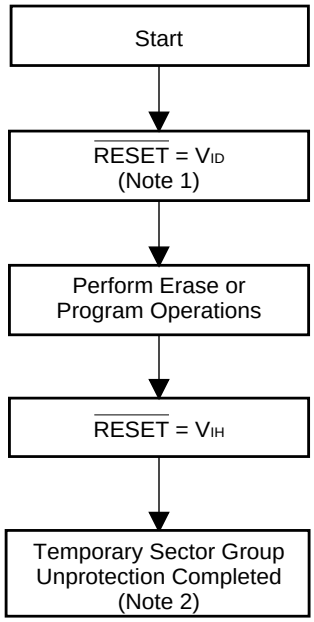


Figure 19 Sector Group Protection Algorithm



Notes:
1. All protected sector groups unprotected.
2. All previously protected sector groups are protected once again.

Figure 20 Temporary Sector Group Unprotection Algorithm

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Sector Erase Time	—	1	15	sec	Excludes 00H programming prior to erasure
Byte Programming Time	—	8	2000	µs	Excludes system-level overhead
Chip Programming Time	—	16	50	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	1,000,000	—	Cycles	

■ TSOP PIN CAPACITANCE

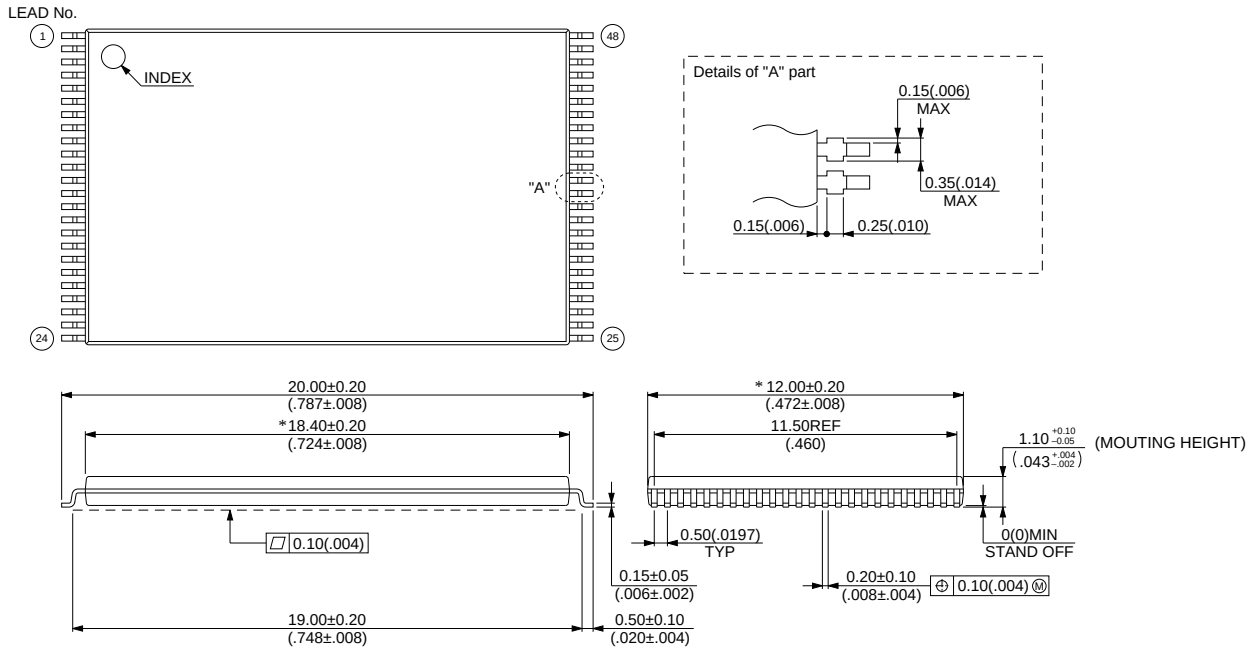
Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Note:
Test conditions T_A = 25°C, f = 1.0 MHz

■ PACKAGE DIMENSIONS

48-Pin Standard Thin Small Outline Package

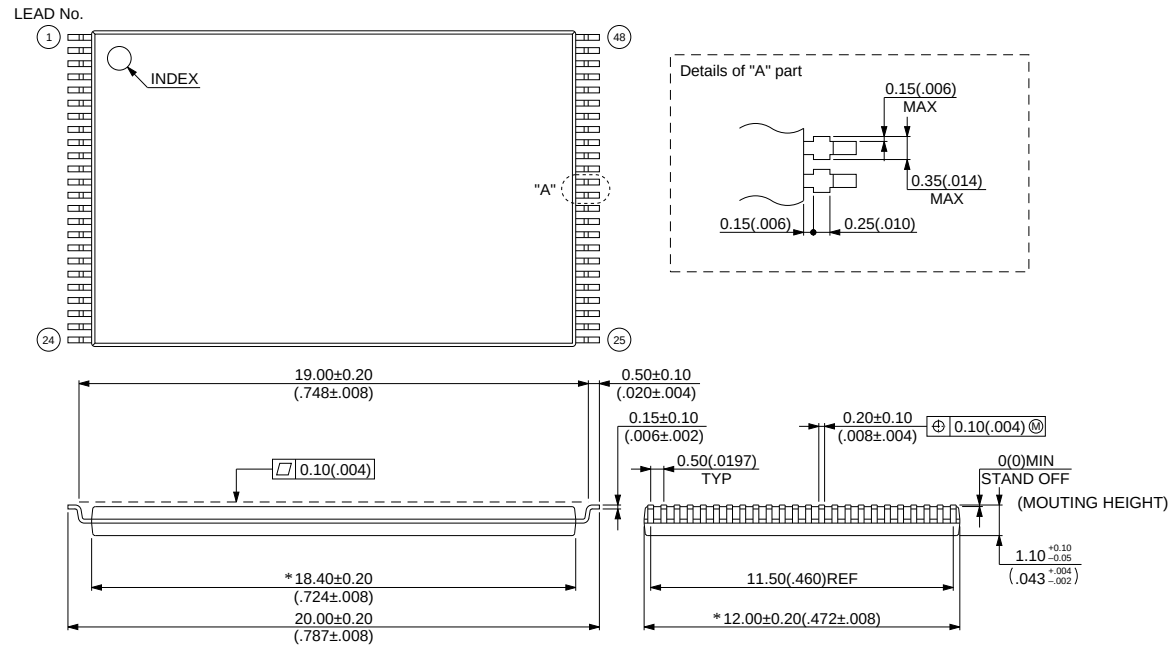
* Resin Protrusion.(Each side: 0.15(.006)MAX)



Dimensions in mm (inches)

48-Pin Reversed Thin Small Outline Package

* Resin Protrusion.(Each side: 0.15(.006)MAX)



Dimensions in mm (inches)

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